AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions and listings of claims in the application:

LISTING OF CLAIMS:

1. (Currently Amended) A ~~D~~digital to analog converter circuit, ~~wherein the digital to analog converter is implemented by~~comprising:

~~two or more~~ a plurality of digital to analog converters whose outputs form different but simultaneous portions of an output of said digital to analog converter circuit~~, in that it is furthermore implemented in such a way that the operation of its analog output voltages is combined and in that its~~; and

a distribution circuit for distributing digital input values of said digital to analog converter circuit~~are processed in~~ to said plurality of D/A converters such ~~a way~~ that, in the case of a continuous incrementing or decrementing of said input values, the individual input values of the ~~two or more~~ plurality of digital to analog converters are incremented or decremented in turn.

2. (Withdrawn) Phase control circuit, comprising a phase detector, a control-circuit filter and a voltage-controlled oscillator, in which the phase detector is constructed in such a way that it compares the phase of the output signal of the voltage-controlled oscillator with the phase of an input signal and delivers an error signal that corresponds to the difference between the two phases, and in which the control-circuit filter is constructed in such a way that it converts the error signal into a control signal for the voltage-controlled oscillator in such a way that the latter

is able to follow both the dynamic fluctuations of the phase of the input signal and also long-term variations in this phase, wherein the control-circuit filter comprises two parallel branches of which a first branch is dimensioned with regard to the dynamic fluctuations and a second branch is dimensioned with regard to the long-term variations.

3. (Withdrawn) Phase control circuit according to Claim 2, characterized in that the first branch is constructed in analog circuit engineering and the second branch is constructed in digital circuit engineering.

4. (Withdrawn) Phase control circuit according to Claim 3, characterized in that the second branch has a window comparator, a counter and a digital to analog converter, wherein the inputs of the digital to analog converter are connected to the outputs of the highest-value stages of the counter.

5. (Withdrawn) Phase control circuit according to Claim 4, characterized in that the number of stages of the counter is dimensioned with regard to the upper cutoff frequency to be ensured by the second branch.

6. (Withdrawn) Phase control circuit according to Claim 4, characterized in that the digital to analog converter is a digital to analog converter, wherein the digital to analog converter is implemented by two or more digital to analog converters, in that it is furthermore implemented

in such a way that the operation of its analog output voltages is combined and in that its digital input values are processed in such a way that, in the case of a continuous incrementing or decrementing of said input values, the individual input values of the two or more digital to analog converters are incremented or decremented in turn.

7. (Withdrawn) Phase control circuit according to Claim 4, characterized in that the window comparator is constructed in such a way that it is capable of having three output states, wherein a first output state is assumed if the input signal of the window comparator lies within a specified narrow range around a setpoint value, that a second output state is assumed if the input signal of the window comparator exceeds the specified narrow range in the one direction, and that a third output state is assumed if the input signal of the window comparator exceeds the specified narrow range in the other direction.

8. (Withdrawn) Phase control circuit according to Claim 2, characterized in that it is furthermore constructed in such a way that it feeds to the phase detector as input signal a data signal to whose data clock pulse the phase of the output signal of the voltage-controlled oscillator is to be adjusted.

9. (Withdrawn) Phase control circuit according to Claim 2, characterized in that, depending on the nature of a third parallel-connected branch, a pre-adjustable voltage source is connected.

10. (Withdrawn) Transmission unit, in particular signal regenerator at the junction between electrical signals and optical signals, having an input circuit for largely restoring a signal trace unaffected by transmission interferences, wherein the input circuit has a phase control circuit according to Claim 6.

11. (Withdrawn) Recognition circuit for recognizing the locking-in of a phase control circuit comprising a phase detector, a control-circuit filter and a voltage-controlled oscillator, in particular a phase control circuit according to Claim 6, wherein the recognition circuit is constructed in such a way that it is capable of impressing an interference variable on the phase control circuit, in that it is furthermore constructed in such a way that it is capable of recognizing a change in the output frequency of the voltage-controlled oscillator, and in that it is furthermore constructed in such a way that it is capable of delivering an alarm signal if impressing an interference variable results in a change in the output frequency.

12. (Withdrawn) Recognition circuit according to Claim 11, characterized in that it is further constructed in such a way that the change in the output frequency of the voltage-controlled oscillator is recognized by means of a frequency counter.

13. (New) A digital to analog converter circuit according to claim 1, wherein said distribution circuit comprises a divide-by-n counter responsive to said input values of said

converter circuit to provide n counter outputs, and n further counters each responsive to a respective one of said n counter outputs, an output from each of said n counters being coupled to a respective one of said plurality of D/A converters.

14. (Currently Amended) A digital to analog converter circuit, comprising:

a plurality of digital to analog converters whose outputs collectively form an output form an output of said digital to analog converter circuit; and

a distribution circuit for distributing digital input values of said digital to analog converter circuit to said plurality of D/A converters such that, in the case of a continuous incrementing of said input values by a given increment amount, the individual input values of the plurality of digital to analog converters are incremented in turn by said given increment amount.

15. (New) A digital to analog converter circuit according to claim 14, wherein said distribution circuit comprises a divide-by-n counter responsive to said input values of said converter circuit to provide n counter outputs, and n further counters each responsive to a respective one of said n counter outputs, an output from each of said n counters being coupled to a respective one of said plurality of D/A converters.